

**PROGRAMMABLE FEEDBACK DELAY PHASE-LOCKED LOOP
FOR HIGH-SPEED INPUT/OUTPUT TIMING BUDGET MANAGEMENT
AND METHOD OF OPERATION THEREOF**

ABSTRACT OF THE DISCLOSURE

A phase-locked loop (PLL), a method of programmably adjusting a phase of a reference clock signal and a synchronous sequential logic circuit incorporating the PLL or the method. In one embodiment, the PLL includes: (1) a digital feedback delay line having a plurality of taps and (2) tap selection logic, coupled to the digital feedback delay line, for activating one of the plurality of taps and thereby insert a corresponding delay into the PLL.